Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – SUMMER 2016

Subject Code:130902 Date:31/05/2016

Subject Name:Analog and Digital Electronics

Time:10:30 AM to 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Discuss Slew Rate with reference to 741C op-amp.	**07**
	(b)	State and prove De Morgan's theorems.	**07**
Q.2	**(a)**	Write short note on nand gate R-S flip flop.	**07**
	(b)	Write short note on J-K flip flop.	**07**
		OR	
	(b)	Write short note on Edge triggering of flip-flop.	**07**
Q.3	**(a)**	With suitable example explain binary addition, subtraction, division and multiplication.	**07**
	(b)	Explain astable mode of operation of 555 timer.	**07**
		OR	
Q.3	**(a)**	Explain application of op-amp as integrator and differentiator.	**07**
	(b)	What are demerits of open loop configuration of op-amp? How can we overcome this?	**07**
Q.4	**(a)**	Explain Full adder and Half adder circuit	**07**
	(b)	Explain three variables and four variables K-map.	**07**
		OR	
Q.4	**(a)**	Explain AND and OR gate using diode and transistor circuit.	**07**
	(b)	Explain three pin voltage regulator IC. Explain LM 78XX and LM 79XX.	**07**
Q.5	**(a)**	How can be obtained 1's and 2's compliment of binary number?	**07**
	(b)	Describe the working of look-ahead-carry adder.	**07**
		OR	
Q.5	**(a)**	Explain working of counter and register.	**07**
	(b)	Explain Multiplexer and De-multiplexer.	**07**

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