

**GUJARAT TECHNOLOGICAL UNIVERSITY****BE - SEMESTER-III (OLD) EXAMINATION – WINTER 2018****Subject Code:130902****Date:22/11/2018****Subject Name:Analog And Digital Electronics****Time:10:30 AM TO 01:00 PM****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Explain block diagram of Op-Amp with function of each block. What are the ideal characteristics of an Op-Amp. **07**
- (b) Why NAND gate and NOR gate are known as universal gate? Obtain AND, OR and NOT gate using NAND and NOR gate. **07**
- Q.2** (a) Draw functional block diagram of IC 555 & discuss function of each pin. **07**
- (b) Enlist the applications of 555 timer in astable and monostable mode. **07**
- OR**
- (b) Explain the working of IC 555 as a bistable multivibrator. **07**
- Q.3** (a) Explain the working of Op-Amp as differentiator. **07**
- (b) Explain with the truth table, the working of R-S flip flop. **07**
- OR**
- Q.3** (a) Explain inverting and non-inverting amplifier using Op-Amp. **07**
- (b) Explain with the truth table, the working of J-K flip flop. **07**
- Q.4** (a) What is a Multiplexer? Explain with diagram and truth table the operation of 4:1 Multiplexer. **07**
- (b) With the help of neat circuit diagram explain the working of a two input TTL NAND gate. **07**
- OR**
- Q.4** (a) What is Decoder? Draw truth table and logic diagram of 3 to 8 line Decoder. Give difference between Decoder and Demultiplexer. **07**
- (b) With the help of neat circuit diagram explain the working of a two input CMOS NOR gate. **07**
- Q.5** (a) What is the basic difference between synchronous and asynchronous counter? Explain 3-bit asynchronous up counter using T flip-flop. **07**
- (b) Explain the working of Master-Slave J-K flip-flop **07**
- OR**
- Q.5** (a) Give classification of registers. Discuss 4 – bit buffer register using D – flip flop. **07**
- (b) Derive full adder with the help of necessary truth table, K-map. Also express in AOI logic diagram. **07**

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