Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(New) • EXAMINATION – WINTER 2016

Subject Code:2131004 Date:06/01/2017

Subject Name:Digital Electronics

Time:10:30 AM to 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Do as directed.**	**14**
	1	$(56)_{16} = (?)_{10}$	
	2	$(32)_{10} = (?)_{2}$	
	3	Bubbled OR gate is also called_____.	
	4	Define: Fan in	
	5	Define: Noise Margin	
	6	Design a NOT gate using a two input Ex-OR gate.	
	7	Which logic family is the fastest logic family?	
	8	Why ROMs are called nonvolatile memory?	
	9	What is the significance of the *J* and *K* terminals on the J-K flip-flop? (a) There is no known significance in their designations. (b) The *J* represents "jump," which is how the *Q* output reacts whenever the clock goes high and the *J* input is also HIGH. (c) The letters were chosen in honor of Jack Kilby, the inventory of the integrated circuit. (d) All of the other letters of the alphabet are already in use.	
	10	How many inputs are required for a 1-of-16 decoder? (a) 2 (b) 4 (c) 8 (d) 12	
	11	State the distributive property of Boolean algebra.	
	12	Which logic family consumes the less power?	
	13	Define : Negative Logic	
	14	How many flip fops are required to count the sequence from 0 to 63?	
Q.2	**(a)**	Why NAND gate is known as universal gate?	**03**
	(b)	Find the 10's complement of the following: (1) $(935)_{11}$ (2) $(6106)_{10}$	**04**
	(c)	Design 3-bit parity generator circuit using even parity bit.	**07**
		OR	
	(c)	Using D as the VEM, reduce Y=A′B′C′D′+A′B′CD′+AB′C′D′+AB′C′D+AB′CD′+AB′CD.	**07**
Q.3	**(a)**	Obtain the truth table of the function: F= xy + xy′ + y′z.	**03**
	(b)	Explain RS flip flop in detail.	**04**
	(c)	Explain full adder and design a full adder circuit using 3 to 8 decoder and two OR gates.	**07**
		OR	
Q.3	**(a)**	Design one bit magnitude comparator.	**03**
	(b)	Implement the given function using multiplexer. F (A, B, C) = Σ (1, 3, 5, 6)	**04**
	(c)	Design BCD to Excess-3 code convertor circuit.	**07**
Q.4	**(a)**	Show that (A + C) (A + D) (B + C) (B + D) = AB + CD	**03**
	(b)	Explain Moore machine.	**04**
	(c)	Design Modulo-8 counter using T flip flop.	**07**

OR

Q.4	**(a)**	Explain edge triggering and level triggering.	**03**
	(b)	Explain 4 bit serial in serial out shift register.	**04**
	(c)	Design 3-bit synchronous up counter using T flip flop.	**07**
Q.5	**(a)**	Give classification of logic families. Also list the characteristics of digital IC.	**03**
	(b)	Explain Half Adder circuit with neat diagram.	**04**
	(c)	Write short note on Read Only Memory (ROM).	**07**

OR

Q.5	**(a)**	What is race around condition in JK flip flop.	**03**
	(b)	How does a counter works as frequency divider? Explain with suitable example.	**04**
	(c)	A combinational logic circuit is defined by the functions: $F_1 = \Sigma (3, 5, 6, 7)$ and $F_2 = \Sigma (0, 2, 4, 7)$. Implement the circuit with a PLA having three inputs, four product terms and two outputs.	**07**

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