

Seat No.: _____

Enrolment No. _____

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER-III (NEW) - EXAMINATION – SUMMER 2018****Subject Code:2131004****Date:25/05/2018****Subject Name:Digital Electronics****Time:10:30 AM to 01:00 PM****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

		MARKS
Q.1	(a) Implement NOT, AND, & OR gates using NAND gates only.	03
	(b) State & prove De Morgan's theorems with the help of truth tables.	04
	(c) Draw the truth tables for JK & T FF. Using these truth tables, derive & explain the excitation tables of JK & T FF.	07
Q.2	(a) Convert 1000 0110 (BCD) to decimal, binary & octal.	03
	(b) Convert 33.45_{10} to binary. Result should be accurate to within 0.01_{10} .	04
	(c) i. Using laws of Boolean algebra prove that $AB + BC + A'C = AB + A'C$.	07
	ii. Minimize the logic function $X = A(B' + C')(A + D)$. Also realize the reduced function using NOR gates only.	
	OR	
	(c) i. Reduce to simplest form using K-map: $F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$	07
	ii. Using D as the MEV, reduce $Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + A\bar{B}C\bar{D} + A\bar{B}C\bar{D}$.	
Q.3	(a) Draw logic circuit of 4:1 MUX.	03
	(b) Design 3-bit even parity generator circuit using X-OR gates only.	04
	(c) Realize the expression $Y(A, B, C, D) = \Sigma m(15, 7, 4, 6, 8, 9, 12, 14)$ using an 8:1 MUX.	07
	OR	
Q.3	(a) Design 1-bit magnitude comparator circuit.	03
	(b) Draw logic diagram of 3-line to 8-line decoder.	04
	(c) Using suitable decoder & OR gates, design 4-bit binary to Gray code converter.	07
Q.4	(a) Draw high assertion & low assertion input SR latches.	03
	(b) Design 3-bit ripple up-counter using negative edge triggered JK flip flops. Also draw the waveforms.	04
	(c) Design a counter to generate the repetitive sequence 0, 3, 5, 7, 4 using D FFs.	07

OR

- Q.4** (a) Draw gated SR latch using NAND gates only. **03**
(b) Make comparison: **04**
 i. ROM vs PLA
 ii. PLA vs PAL
(c) Explain the output glitch problem generated due to different switching speed of the FFs. Also explain state assignment to eliminate glitches with the help of suitable example & necessary diagrams. **07**
- Q.5** (a) How many FFs are required to design FSM with 100 states? Give calculation. **03**
(b) Compare TTL, ECL, & CMOS logic families. **04**
(c) List out problems of asynchronous circuit. Also exemplify any two problems with suitable examples. **07**
- OR**
- Q.5** (a) List out various logic families. Also list the characteristics of digital ICs. **03**
(b) Draw and explain 4-bit serial-in serial-out shift register using D FFs. **04**
(c) Using 8x4 ROM, realize the expressions $F1 = AB'C + ABC' + A'BC$, $F2 = A'B'C + A'BC' + AB'C'$, $F3 = A'B'C' + ABC$. Show the contents of all locations. **07**
