

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER-III (New) EXAMINATION – WINTER 2018****Subject Code: 2131004****Date:05/12/2018****Subject Name: Digital Electronics****Time:10:30 AM TO 01:00 PM****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

		MARKS
Q.1	(a) Convert the following numbers form given base to the base indicates.	03
	1. $(AEF2.B6)_{16} = (\text{_____})_2$	
	2. $(674.12)_8 = (\text{_____})_{10}$	
	3. $(110110.1011)_2 = (\text{_____})_{16}$	
	(b) Solve the following Boolean functions by using K-Map. Implement the simplified function by using logic gates	04
	$F = (w,x,y,z) = \Sigma (0,1,4,5,6,8,9,10,12,13,14)$	
	(c) With a neat block diagram explain the function of encoder. Explain priority encoder?	07
Q.2	(a) Define State Machine	03
	(b) Discuss Clocked R-S Flip-flop with Logic diagram, Symbol, Characteristic table and Characteristic equation	04
	(c) Design a counter for following binary sequence 0-1-3-4-6-0.	07
OR		
	(c) Implement the following Boolean functions with a multiplexer and Decoder.	07
	$F(w, x, y, z) = \Sigma (2, 3, 5, 6, 11, 14, 15)$	
Q.3	(a) What is “Lock out” condition in counter? How to avoid it.	03
	(b) List down the various types of ROMs and discuss and two of them.	04
	(c) With suitable design example discuss the basic design principles of Asynchronous State Machines design.	07
OR		
Q.3	(a) Draw the Characteristic tables of following Flip-flop.	03
	1. R-S 2. J-K 3. T	
	(b) Design a combinational logic circuit whose output is high only when majority of inputs (A, B, C, D) are low.	04
	(c) Implement the following function with NAND and NOR Gate.	07
	$F(a,b,c) = \Sigma (0,6)$	
Q.4	(a) Discuss the advantages and disadvantages of TTL Logic Family.	03
	(b) List down the modes of Asynchronous Sequential Machine and discuss any one in detail.	04
	(c) Determine the minimum state table equivalent shown in following table and draw the reduce state diagram.	07

q	X=0		X=1	
	N.S.	O/P	N.S.	O/P
1.	1	0	1	0
2.	1	1	6	1
3.	4	0	5	0
4.	1	1	7	0
5.	2	0	3	0
6.	4	0	5	0
7.	2	0	3	0

OR

- Q.4** (a) State and prove DeMorgan Theorem. **03**
 (b) Explain Serial Transfer w.r.t Shift Register with suitable example. **04**
 (c) Design a 3-bit gray to binary code converter. Implement it using suitable PROM. Draw the necessary diagrams and tables. **07**
- Q.5** (a) Explain following terms w.r.t Digital Logic Family. **03**
 1. Fan-in 2.Noise Margin 3. Power Dissipation
 (b) Simplify the following Boolean functions to a minimum numbers of literals. **04**
 1. $x + x'y$ 2. $x(x'+y)$ 3. $x'y'z + x'yz + xy'$ 4. $xy + x'z + yz$
 (c) Design a 3-bit binary counter. **07**

OR

- Q.5** (a) Define following terms w.r.t State Machine. **03**
 1. State Table 2. State Diagram.
 (b) Describe General State Machine Architecture with suitable diagrams. **04**
 (c) Which are the various problems of Asynchronous Circuits? Explain any four in detail. **07**
