

**GUJARAT TECHNOLOGICAL UNIVERSITY****ME - SEMESTER– I (New course)• REMEDIAL EXAMINATION – SUMMER 2015****Subject Code: 3715201****Date:12/05/2015****Subject Name: Advanced Computer Architecture****Time: 10:30 am to 1:00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

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|------------|---|-----------|
| <b>Q.1</b> | (a) What are Classes of Computer architecture   | <b>07</b> |
|            | (b) Explain about Processor vs. System architecture   | <b>07</b> |
| <b>Q.2</b> | (a) Explain Data Hazard in detail.  | <b>07</b> |
|            | (b) Explain the below mentioned concepts and differentiate them.<br>1.RISC and CISC<br>2. Big-endian and Little-endian. | <b>07</b> |
| <b>OR</b>  |   |           |
|            | (b) Describe in brief Interrupt Controller MPCore processors  | <b>07</b> |
| <b>Q.3</b> | (a) Explain 3 stage pipeline in ARM architecture  | <b>07</b> |
|            | (b) Explain Host Interface for GPU  | <b>07</b> |
| <b>OR</b>  |   |           |
| <b>Q.3</b> | (a) Draw block diagram of Unified instruction and data cache  | <b>07</b> |
|            | (b) Explain SIMD instructions in brief.   | <b>07</b> |
| <b>Q.4</b> | (a) Draw block diagram of Harvard architecture based data and instruction caches  | <b>07</b> |
|            | (b) List advantages & disadvantages of Onchip RAM   | <b>07</b> |
| <b>OR</b>  |   |           |
| <b>Q.4</b> | (a) Explain Paging memory management to MMU   | <b>07</b> |
|            | (b) Explain memory Segmentation in brief  | <b>07</b> |
| <b>Q.5</b> | (a) Explain vertex processing in GPU  | <b>07</b> |
|            | (b) Describe a typical Typical TLB Format   | <b>07</b> |
| <b>OR</b>  |   |           |
| <b>Q.5</b> | (a) What are Implications for Compilers design in VLIW.   | <b>07</b> |
|            | (b) What are essential components of a toolchain and explain each.  | <b>07</b> |

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