

**GUJARAT TECHNOLOGICAL UNIVERSITY****ME - SEMESTER– I (New course)• REMEDIAL EXAMINATION – SUMMER 2015****Subject Code: 3715501****Date:12/05/2015****Subject Name: Advanced Computer Architecture****Time: 10:30 am to 1:00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

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|------------|--|-----------|
| <b>Q.1</b> | <b>(a)</b> Explain various classes of computer architecture.                               | <b>07</b> |
|            | <b>(b)</b> Explain Memory Hierarchy.   | <b>07</b> |
| <b>Q.2</b> | <b>(a)</b> Compare various platforms in terms of performance and efficiency.               | <b>07</b> |
|            | <b>(b)</b> Explain subroutine nesting and the processor stack.                             | <b>07</b> |
|            | <b>OR</b>  |           |
|            | <b>(b)</b> Explain handling of multiple devices.   | <b>07</b> |
| <b>Q.3</b> | <b>(a)</b> Explain Pipeline Organization in detail.  | <b>07</b> |
|            | <b>(b)</b> Explain various addressing modes in instruction set architecture.               | <b>07</b> |
|            | <b>OR</b>  |           |
| <b>Q.3</b> | <b>(a)</b> Compare and contrast RISC v/s CISC.   | <b>07</b> |
|            | <b>(b)</b> Explain Cache Coherency.  | <b>07</b> |
| <b>Q.4</b> | <b>(a)</b> Explain ARM characteristics and register ARM register structure.                | <b>07</b> |
|            | <b>(b)</b> Explain hardware component selection and datasheet analysis.                    | <b>07</b> |
|            | <b>OR</b>  |           |
| <b>Q.4</b> | <b>(a)</b> Explain memory organization and register structure of Intel IA-32 architecture. | <b>07</b> |
|            | <b>(b)</b> Explain application of specific processor for microcontrollers.                 | <b>07</b> |
| <b>Q.5</b> | <b>(a)</b> Explain application of specific processor for multimedia.                       | <b>07</b> |
|            | <b>(b)</b> Explain virtual memory.   | <b>07</b> |
|            | <b>OR</b>  |           |
| <b>Q.5</b> | <b>(a)</b> Explain asynchronous bus organization.  | <b>07</b> |
|            | <b>(b)</b> Explain boot strapping process.   | <b>07</b> |

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