Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

MCA - SEMESTER– 1 EXAMINATION – WINTER 2018

Subject Code: 2610004 Date: 08-01-2019

Subject Name: Fundamentals of Computer Organization

Time: 10.30 am to 1.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Do as Directed. **07**

(1) "CPU is brain of Computer" – Justify.
(2) State truth table for NOR gate.
(3) State major components of a typical digital computer.
(4) What is the Base of Binary number system and Hexadecimal Number system?
(5) $(1010100.01)_2 – (110000.10)_2$ = _____.
(6) Derive dual of X .(X' +Y) = X . Y
(7) State difference between RAM and ROM.

(b) Write a short note on following : **07**

(1) Scanner
(2) RS flip flop

Q.2 **(a)** Do as Directed. **07**

(1) Convert $(ACD1)_{16}$ into Octal Number. Specify the steps you use for conversion.
(2) $(10001)_2 – (11100)_2$ using 1's compliment method.
(3) What is Karnaugh map?
(4) Convert decimal Number (201) into Octal number.
(5) How can you use complement to represent a negative number? Give an example.
(6) Perform : 209.7 – 181.2 using 9's complement method.
(7) Convert $(101101111010)_2$ to its equivalent hexadecimal number.

(b) Explain Indirect and Relative Addressing mode with suitable example. **07**

OR

(b) Explain working of 3-bit counter. **07**

Q.3 **(a)** Write a Boolean expression SOP form for a 3-input A,B,C gating network that will have outputs 1 for designation m0, m1, m3, m6 and m7 and the outputs are 0 for designation m2, m4 and m5. Draw two level NAND to NAND gate combination network for SOP that corresponds to the simplified expression. **07**

(b) Explain design of Full – Adder. **07**

OR

Q.3 **(a)** What is Flip-Flop? Explain how a JK Flip Flop is made from an RS Flip Flop. **07**

(b) What is universal gate? Which gates are known as universal gate? Explain with Reason, use any one such gate as universal gate. **07**

Q.4 **(a)** What is a Multiplexer? Explain 4-to-1 line multiplexer. **07**

	(b)	What is Bus? Explain Address Bus, Data Bus and Control Bus.	**07**
		OR	
Q.4	**(a)**	Explain Direct and Indexed Addressing mode with suitable example.	**07**
	(b)	What is Cache memory and Virtual memory? Explain in detail.	**07**
Q.5	**(a)**	Describe zero-address and two-address instruction word formats.	**07**
	(b)	Explain working of ADD, SUB and NOT instructions with example.	**07**
		OR	
Q.5	**(a)**	Explain Instruction and Execution Cycle.	**07**
	(b)	Explain instruction format of 8086 microprocessor.	**07**

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